CLAIMS INCLUDING REFERENCE SIGNS:

1. Phase detector for detecting a phase between a first input signal (CLK) and a second input signal (REF), characterized in that said phase detector comprises a difference establisher (1) for establishing differences between said input signals and comprises a selector (2) for selecting one of said differences to be an output signal.

2. Phase detector according to claim 1, characterized in that said selector (2) is a feedbackless selector (2).

3. Phase detector according to claim 2, characterized in that said selector (2) comprises latches (21,22) clocked by said second input signal (REF) and for receiving said first input signal (CLK) and for generating latch signals and comprises a multiplexer (23) controlled by said second input signals and for receiving said latch signals and for generating a selection signal.

4. Phase detector according to claim 1, characterized in that said phase circuit comprises a converter (3) for converting said input signals into compensated input signals.

5. Phase detector according to claim 4, characterized in that said converter (3) comprises per input signal a buffer circuit (31,33) coupled to a replica circuit (32,34).

6. Phase detector according to claim 4, characterized in that said difference establisher (1) comprises a subtracting circuit (11) for subtracting compensated input signals from each other and generating a result signal and comprises a modulus circuit (12) for generating moduli of said result signal, with said phase detector comprising a multiplexer (13) to be controlled by a selection signal for selecting a modulus.

7. Phase detector according to claim 4, characterized in that said difference establisher (1) comprises a subtracting circuit (11) for subtracting compensated input signals from each other and generating a result signal and comprises a squaring circuit (12') for

generating squares of said result signal, with said phase detector comprising a multiplexer (13) to be controlled by a selection signal for selecting a square.

8. Phase Locked Loop comprising a phase detector for detecting a phase between a first input signal and a second input signal, characterized in that said phase detector comprises a difference establisher (1) for establishing differences between said input signals and comprises a selector (2) for selecting one of said differences to be an output signal.

9. Method for detecting a phase between a first input signal and a second input signal, characterized in that said method comprises the step of establishing differences between said input signals and the step of selecting one of said differences to be an output signal.

10. Processor program product for detecting a phase between a first input signal and a second input signal, characterized in that said processor program product comprises the function of establishing differences between said input signals and the function of selecting one of said differences to be an output signal.